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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,725	11/13/2003	Lane Thomas Holloway	AUS920030181US1	2699

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SAVLA, ARPAN P	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 12/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,725	HOLLOWAY ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *13 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/713725 has a total of 15 claims pending in the application, there are 3 independent claims and 12 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character is not mentioned in the description: "Super I/O Controller 223." Also, the drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference signs are mentioned in the description: "additional memory 224" and "dotted line 232." Finally, the drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "214" has been used to designate both "expansion bus interface" (detailed description) and "FSP Processor" (drawings), reference character "220" has been used to designate both "mouse adapter" (detailed description) and "FSP

Flash Memory" (drawings), and reference character "222" has been used to designate both "modem" (detailed description) and "NVRAM" (drawings).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by Examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. As required by MPEP § 609(c), Applicant's submission of the Information Disclosure Statement dated November 13, 2003 is acknowledged by Examiner and cited references have been considered in the examination of the claims now pending.

As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant office action.

OBJECTIONS

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Method And System For Dynamically Storing Frequently Used Instructions Using A Separate Cache."

5. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The subject matter in question is the instruction in the stack being "accessed again" and also "moved up the stack." When an instruction is accessed from a stack it must be at the top of the stack and then popped of the stack in order to be read. For the instruction to be "accessed again" it must first be re-pushed onto the stack, then be at the top of the stack again, and finally popped off once again to be read. Also, as stated earlier, anytime an instruction is accessed it must be popped off the stack. Therefore, it is not possible the instruction can be "moved up in the stack" after an access because it is no longer on the stack. However, Applicant's specification does not disclose these necessary steps of pushing and popping instructions on and off the stack respectively in a way that one of ordinary skill in the art could ascertain how the claimed invention functions.

6. On page 2, line 17 the phrase "use can" should read "use that can."

7. On page 9, line 3 the phrase "the each line" should read "each line."

8. On page 9 the phrases "counters 308A-C" on lines 22 and 25 should read "counters 308A-G."

9. On page 9 the phrases "line 306A-C" on lines 23 and 24 should read "line 306A-G."

10. On page 15, in the last line the word "holes" should read "holds."

Appropriate correction is required.

Claims

11. **Claim 2 and 4 are objected to because of the following informalities:**

On line 4 of the phrase "all other counters of the **first** plurality are decremented" should read "all other counters of the **second** plurality are decremented." Examiner interprets the claim language as such because of pg. 15, paragraph 2 of the specification and also because claims 8 and 13 are similar and both read "all other counters of the **second** cache are decremented."

12. **As per claim 4**, it is unclear whether the phrase "an instruction" in line 3 is from "a first plurality of instructions" or "a second plurality of instructions" as stated in claim 1.

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 112

13. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

14. **Claims 4, 9, and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.** The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The subject matter in question is the instruction in the stack being "accessed again" and also "moved up the stack." When an instruction is accessed from a stack it must be at the top of the stack and then popped of the stack in order to be read. For the instruction to be "accessed again" it must first be re-pushed onto the stack, then be at the top of the stack again, and finally popped off once again to be read. Also, as stated earlier, anytime an instruction is accessed it must be popped off the stack. Therefore, it is not possible the instruction can be "moved up in the stack" after an access because it is no longer on the stack. However, Applicant's specification does not disclose these necessary steps of pushing and popping instructions on and off the stack respectively in a way that one of ordinary skill in the art could ascertain how the claimed invention functions.

15. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

16. **Claims 12-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention**. The claims disclose an "instruction" that is stored in a "second cache." However, neither the "first instruction", "second instruction", "third instruction", nor "fourth instruction" disclosed in claim 11 is ever stored in a "second cache." Examiner believes that for claims 12-14 "instruction" should instead read "line of data" because claim 11 discloses storing a "line of data" in a "second cache." Applicant may consider amending claims 12-14 in order to be consistent with claim 11.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

17. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

18. Claims 1, 3, and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Mendelson et al. (U.S. Patent Application Publication 2002/0095553).

19. **As per claim 1**, Mendelson discloses a cache system for a computer system, comprising:

a first cache for storing a first plurality of instructions (paragraph 0003, lines 9-12; paragraph 0028, lines 4-6; paragraph 0033, lines 2-3; Fig. 1C, elements 101_1 - 101_N;

Fig. 3, element 320). It should be noted that "filter trace cache (FTC)" is analogous to "first cache."

a second cache for storing a second plurality of instructions (paragraph 0028, lines 4-6; Fig. 1C, elements 101_1 - 101_N; Fig. 3, element 330). It should be noted "main trace cache (MTC)" is analogous to "second cache."

wherein each instruction of the first plurality has an associated counter and wherein when a first instruction of the first plurality is accessed, a first associated counter is incremented (paragraph 0031, lines 10-13; Fig. 3, element 360).

and wherein when the first associated counter reaches a threshold, the first instruction of the first plurality is copied into the second cache (paragraph 0034, lines 15-16).

20. **As per claim 3**, Mendelson discloses the first instruction of the first plurality is accessed from the second cache (paragraph 0035, lines 15-16).

21. **As per claim 6**, Mendelson discloses a method of managing cache in a computer system, comprising the steps of:

checking for a first instruction in a first cache, wherein each instruction in the first cache has an associated counter (paragraph 0031, lines 10-11; paragraph 0032, lines 2-3; paragraph 0033, lines 2-3; Fig. 1C, elements 101_1 - 101_N; Fig. 3, elements 320 and 360);

if the first instruction is found in the first cache, incrementing a first associated counter (paragraph 0031, lines 11-13);

comparing a value of the first associated counter to a threshold (paragraph 0034, lines 9-11);

if the first associated counter exceeds the threshold, moving the first instruction from the first cache to a second cache (paragraph 0034, lines 15-16).

22. **As per claim 7**, Mendelson discloses the step of:

accessing the first instruction from the second cache (paragraph 0035, lines 15-17).

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Wickeraad et al. (U.S. Patent Application Publication 2001/0001873).

25. **As per claim 2**, Mendelson discloses all the limitations of claim 2, except each instruction of the second plurality has an associated counter, and wherein when an instruction of the second plurality is accessed, all other counters of the second plurality are decremented.

Wickeraad discloses each instruction of the second plurality has an associated counter, and wherein when an instruction of the second plurality is accessed, all other counters of the second plurality are decremented (paragraph 0013, lines 2-4 and 8-12).

It should be noted that "memory operand" is analogous to "instruction." It should also be noted that if the "memory operand" is loaded into the cache line it is inherently required the "memory operand" was first accessed from main memory.

Mendelson and Wickeraad are analogous art because they are from the same field of endeavor, that being cache replacement techniques.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wickeraad's cache with an associated LRU counter for each cache line within Mendelson's trace cache subsystem.

The motivation for doing so would have been because the algorithm observes both cache hits and cache missed to create correspondence between the cache line selected for replacement and the probability that the cache line will be needed soon, thus, the LRU algorithm tends to be very effective (Wickeraad, paragraph 0012, lines 4-8).

Therefore, it would have been obvious to combine Mendelson and Wickeraad for the benefit of obtaining the invention as specified in claim 2.

26. **As per claim 6**, Wickeraad discloses each instruction of the second cache has an associated counter, and wherein when an instruction of the second cache is accessed, all other counters of the second cache are decremented (paragraph 0013, lines 2-4 and 8-12).

27. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Norman P. Jouppi, Improving Direct-Mapped Cache

Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers, hereafter "Jouppi."

28. **As per claim 5**, Mendelson discloses the first cache is an instruction cache (paragraph 0003, lines 9-12; paragraph 0028, lines 4-6; Fig. 1C, elements 101_1 - 101_N; Fig. 3, element 320).

Mendelson does not expressly disclose the second cache is fully associative and follows a least recently used policy.

Jouppi discloses the second cache is fully associative and follows a least recently used policy (pg. 367, section 3.1, lines 4-8).

Mendelson and Jouppi are analogous art because they are from the same field of endeavor, that being cache replacement techniques.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Jouppi's fully associative miss cache which follows a LRU replacement policy within Mendelson's trace cache subsystem.

The motivation for doing so would have been to have a cache that is fully-associative and has LRU replacement, thus eliminating the occurrences of conflict misses (Jouppi, pg. 366, section 3, lines 3-5).

Therefore, it would have been obvious to combine Mendelson and Jouppi for the benefit of obtaining the invention as specified in claim 5.

29. **As per claim 10**, Mendelson discloses the first cache is an instruction cache (paragraph 0003, lines 9-12; paragraph 0028, lines 4-6; Fig. 1C, elements 101_1 - 101_N; Fig. 3, element 320).

Mendelson does not expressly disclose the second cache is fully associative and follows a least recently used policy.

Jouppi discloses the second cache is fully associative and follows a least recently used policy (pg. 367, section 3.1, lines 4-8).

30. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Andrew S. Tanenbaum, Structured Computer Organization, 2nd Edition, hereafter "Tanenbaum."

31. **As per claim 11**, Mendelson discloses checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter (paragraph 0031, lines 10-11; paragraph 0032, lines 2-3; paragraph 0033, lines 2-3; Fig. 1C, elements 101_1 - 101_N; Fig. 3, elements 320 and 360);

if the first line of data is found in the first cache, incrementing a first associated counter (paragraph 0031, lines 11-13);

comparing a value of the first associated counter to a threshold (paragraph 0034, lines 9-11);

if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache (paragraph 0034, lines 15-16).

Mendelson does not expressly disclose a computer program product in a computer readable medium, comprising:

first instructions for checking for a first line of data in a first cache, wherein each line of data in the first cache has an associated counter;

second instructions for, if the first line of data is found in the first cache, incrementing a first associated counter;

third instructions for comparing a value of the first associated counter to a threshold;

fourth instructions for, if the first associated counter exceeds the threshold, moving the first line of data from the first cache to a second cache.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

Mendelson and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer hardware.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to follow Tanenbaum's argument and implement Mendelson's trace cache subsystem using instructions on a computer program product in a computer-readable medium having (i.e. implement hardware using software).

The motivation for doing so would have been to optimize such factors as cost, speed, and reliability (Tanenbaum, pg. 11, lines 14-15).

Therefore, it would have been obvious to combine Mendelson and Tanenbaum for the benefit of obtaining the invention as specified in claim 11.

32. **As per claim 12**, Mendelson discloses accessing the first instructions from the second cache (paragraph 0035, lines 15-16).

Mendelson does not disclose expressly a computer program, further comprising the step of:

accessing the first instruction from the second cache.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

33. Claim 13 is rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Tanenbaum as applied to claim 11 above, and further in view of Wickeraad.

Mendelson/Tanenbaum discloses all the limitations of claim 13 except each instruction of the second cache has an associated counter, and wherein when an instruction of the second cache is accessed, all other counters of the second cache are decremented.

Wickeraad discloses each instruction of the second cache has an associated counter, and wherein when an instruction of the second cache is accessed, all other counters of the second cache are decremented (paragraph 0013, lines 2-4 and 8-12).

Mendelson/Tanenbaum and Wickeraad are analogous art because they are from the same field of endeavor, that being cache replacement techniques.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Wickeraad's cache with an associated LRU counter for each cache line as software within Mendelson/Tanenbaum's software trace cache subsystem.

The motivation for doing so would have been because the algorithm observes both cache hits and cache missed to create correspondence between the cache line selected for replacement and the probability that the cache line will be needed soon,

thus, the LRU algorithm tends to be very effective (Wickeraad, paragraph 0012, lines 4-8).

Therefore, it would have been obvious to combine Mendelson/Tanenbaum and Wickeraad for the benefit of obtaining the invention as specified in claim 13.

34. Claim 15 is rejected under 35 U.S.C. 103(a) as being obvious over Mendelson in view of Tanenbaum as applied to claim 11 above, and further in view of Jouppi.

35. Mendelson/Tanenbaum discloses the first cache is an instruction cache (paragraph 0003, lines 9-12; paragraph 0028, lines 4-6; Fig. 1C, elements 101_1 - 101_N; Fig. 3, element 320).

Mendelson/Tanenbaum does not expressly disclose the second cache is fully associative and follows a least recently used policy.

Jouppi discloses the second cache is fully associative and follows a least recently used policy (pg. 367, section 3.1, lines 4-8).

Mendelson/Tanenbaum and Jouppi are analogous art because they are from the same field of endeavor, that being cache replacement techniques.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement Jouppi's fully associative miss cache which follows a LRU replacement policy as software within Mendelson/Tanenbaum's software trace cache subsystem.

The motivation for doing so would have been to have a cache that is fully-associative and has LRU replacement, thus eliminating the occurrences of conflict misses (Jouppi, pg. 366, section 3, lines 3-5).

Therefore, it would have been obvious to combine Mendelson/Tanenbaum and Jouppi for the benefit of obtaining the invention as specified in claim 15.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

The following references disclose **cache replacement techniques**.

U.S. Patent Number

5,043,885

6,385,697

6,532,520

U.S. Patent Application Publication Number

2001/0049818

2002/0032840

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, **claims 1-15** have received a first action on the merits and are subject of a first action non-final.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
December 13, 2005

DONALD SPARKS
SUPERVISORY PATENT EXAMINER